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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,303	05/19/2006	Roy Knechtel	60291.000048	7114
21967 7590 12/19/2008 HUNTON & WILLIAMS LLP INTELLECTUAL PROPERTY DEPARTMENT 1900 K STREET, N.W. SUITE 1200 WASHINGTON, DC 20006-1109			EXAMINER PARENDO, KEVIN A	
			ART UNIT 2823	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/595,303

Applicant(s)

KNECHTEL, ROY

Examiner

Kevin Parendo

Art Unit

2823

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 September 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 11-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 11-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
- Paper No(s)/Mail Date 12/7/07 and 9/11/08
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of species I, the embodiment of Figs. 1-2, in the reply filed on 9/11/08 is acknowledged.

While not argued so by the applicant, the examiner believes that the restriction requirement is improper, as this application is a 371 of PCT; as such, any restriction requirement should involve a "unity of invention" standard (see MPEP 1893.03(d)) rather than the "independent or distinct" standard that had been previously applied. Thus, the restriction requirement is withdrawn. Claims 1-9 and 11-20 are pending and will be examined.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because the filed oath is not in English. Thus, it is thus not possible to examine the oath for the various requirements of an oath.

Claim Objections

3. Claim(s) 1, 11, and 20 is/are objected to because it/they contain(s) the limitation "the firm connection" on line 1. This limitation has not been claimed previously to this

instance and thus lacks proper antecedent basis. To avoid any ambiguity, the word "the" should be changed to "a". Appropriate correction is required.

4. Claim(s) 1-9 is/are objected to because claim 1 contain(s) the limitation "processed semiconductor wafers" on lines 1-2, the limitation "more than two wafers" on line 4, the limitation "the wafers" on line 4, the limitation "semiconductor wafers" on line 7, "the limitation "the wafers" on line 12, and the limitation "the wafers" on line 13. These limitations all include the word "wafer," and it is unknown if these limitations all refer to the same wafers or not. The claim language of the above limitations, and any instances of "wafer" in the dependent claims 2-9, must be brought into unambiguous agreement with each other. Appropriate correction is required.

5. Claim(s) 1 is/are objected to because it/they contain(s) the limitation "electrically non-conducting and electrically conducting glass paste" on lines 9-10 that should be amended to "electrically non-conducting glass paste and electrically conducting glass paste". Line 11 contains the limitation "the glass pastes" that lacks proper antecedent basis and that should be amended to "the electrically non-conducting glass paste and the electrically conducting glass paste. Lastly, claim 1 contains the limitation "the glasses of the glass pastes" on lines 13-14 that lacks proper antecedent basis. It appears that it should be amended to "the electrically non-conducting glass paste and the electrically conducting glass paste".

6. Claim(s) 3-4 and 13-14 is/are objected to because it/they contain(s) the limitation "the non-conducting, low melting glass paste" that lacks proper antecedent basis.

Appropriate correction is required.

7. Claim(s) 4, 5, 8, 14, 15, and 18 is/are objected to because it/they contain(s) the limitation "the same processing temperature" (claims 4 and 14), "different processing temperatures" (claims 5 and 15), and "a temperature" (claims 8 and 18). These limitations must be brought into proper agreement with the limitation "processing temperature" in claims 1 and 11.

8. Claim(s) 5 is/are objected to because it/they contain(s) the limitation "the low-melting glass paste" lacks proper antecedent basis. Appropriate correction is required.

9. Claim(s) 8 is/are objected to because it/they contain(s) the limitation "the connections" and the limitation "the glass pastes" on line 2. These limitations have not been claimed previously to this instance and thus lack proper antecedent basis.

Appropriate correction is required.

10. Claim(s) 8 and 18 is/are objected to because it/they contain(s) the limitation "the formation". This limitation has not been claimed previously to this instance and thus lack proper antecedent basis. Appropriate correction is required.

11. Claim(s) 9 and 19 is/are objected to because it/they contain(s) the limitation "characterized in that" that should be amended to "wherein". They also contain the limitation "in particular" that is ambiguous. The limitation "the substrate for SOI wafers" is ambiguous as to whether the substrate is a SOI wafer, or if it is merely a substrate that can have a SOI wafer attached. The limitation "the electric connection... is implemented through previously produced openings in a buried oxide layer and in an active silicon layer" is ambiguous as whether or not the openings are formed in the active silicon layer, or if the electric connection is formed in the active silicon layer. The limitation "the wall areas" has not been claimed before and lacks proper antecedent basis. The limitation "the opening" lacks proper antecedent basis and is ambiguous as to whether it is one of the "previously formed openings". The limitation "the electric connection" on line 2 lacks proper antecedent basis and is ambiguous as to if it is one of the "electrically insulating connections" or one of the "electrically conductive connections" of the independent claims. Appropriate correction is required.

12. Claim(s) 11-19 is/are objected to because claim 11 contain(s) the limitation "processed semiconductor wafers" on lines 1-2, the limitation "system wafer" on line 2, the limitation "cover wafer" on line 3, the limitation "the semiconductor wafers" on lines 5-6, and the limitation "the wafers" on line 11 and line 12. These limitations all include the word "wafer," and it is unknown if these limitations all refer to the same wafers or not. The claim language of the above limitations, and any instances of "wafer" in the

dependent claims 12-19, must be brought into unambiguous agreement with each other. Appropriate correction is required.

13. Claims 4 and 14 are objected to because the term "substantially" is a relative term (one definition of "substantial" is "being largely but not wholly that which is specified") that renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "a process for the firm connection of processed semiconductor wafers, wherein, in the case of more than two wafers, the wafers located in a central area of the stack and wherein in an operation of a mechanically firm connecting electrical insulating connections (6, 6a, 6b) and electrically conductive connections (5) are produced between the semiconductor wafers" on lines 1-7. The

metes and bounds of the claimed limitation can not be determined for the following reasons: this limitation fragment after "more than two wafers" is a run-on that makes it ambiguous as to what the limitation means. It is unknown if this limitation issues a conditional case that there could be only two wafers, but if there are more than two wafers, they must be in the central area of the stack. Thus, it is unknown how many wafers are required.

Also, it is unknown if "semiconductor wafers", "the wafers", "more than two wafers", and "processed semiconductor wafers" all refer to the same wafers, or if some limitations refer to the same set of wafers while other limitations refer to other wafers.

The claim has the limitation "the two wafer sides to be connected with each other"; this further makes it ambiguous as to how many wafers there are, as if there are only two sides being connected, it is unknown how there could be "more than two wafers."

Lastly, claim 1 recites the limitation "applying structured layers of electrically non-conducting and electrically conducting glass paste on respectively one of the two wafer sides". The meaning of this limitation is unclear. First, it is unknown what a "structured layer" is. It could mean that it is one layer that is made of "sub-layers" of the two types of paste, but it could also mean that it is a layer that has "structures" in it. Also, "respectively" means "separately;" a sentence such as "Sara and Brad are respectively eight and ten years old" means that Sara is eight years old and Brad is ten years old. It is unknown how two pastes can be up on "respectively one" side. Thus, it is unknown which paste(s) is formed on which side(s) of the "two wafer sides".

Claims 2-9 depend from claim 1, and thus require the same limitations as listed above, and thus are also rejected as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. See MPEP § 2173.05(c). Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949). In the present instance, claim 2 recites the broad recitation "glass paste", and the claim also recites "in particular glass solder applied with a screen printing process" which is the narrower statement of the range/limitation.

Also, claim 2 recites the limitation "glass solders". The metes and bounds of the claimed limitation can not be determined for the following reasons: it is unknown, and would not be clear to one of ordinary skill in the art, what a "glass solder" is. As supported by the "solder" entry from the Academic Press Dictionary of Science and Technology, a solder is an alloy used to join metal objects; an alloy is metallic, not glass. Thus, it is unclear what this limitation refers to, and it appears that the word "solder" has been used incorrectly. The specification contains no enlightening information regarding this issue.

16. Claims 3 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3 and 13 recite the limitation "the glass pastes, in particular glass solders are applied with a screen printing process." The metes and bounds of the claimed limitation can not be determined for the following reasons: it is unknown if the glass pastes are limited to be glass solders.

17. Claims 3 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3 and 13 recite the limitation "the conditioning and premelting are implemented successively in a respectively separate process." The metes and bounds

of the claimed limitation can not be determined for the following reasons: it is unknown how a single "respectively separate process" can be implemented "successively" or how it can be referred to as "respectively" when it is a single process and it appears that the conditioning and premelting are intended to be two separate processes.

18. Claims 6 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 6 and 16 recite the limitation "not structured electronically as an (area of the starting material)." The metes and bounds of the claimed limitation can not be determined for the following reasons: the meaning of this limitation is unknown. "The starting material" has not been claimed previously, and it is unknown to what this refers. It is also unclear as to why there are parentheses in this limitation.

19. Claims 11-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 recites the limitation "for the firm connection of processed semiconductor wafers as system wafer (1) supporting microelectromechanical or electronic structures with a cover wafer (2) also supporting electronic structures, wherein in an operation of a mechanically firm connecting electrically insulating connections and electrically conductive connections are produced between the

semiconductor wafers" " on lines 1-6. The metes and bounds of the claimed limitation can not be determined for the following reasons: this limitation is a run-on that makes its meaning ambiguous. It is unclear what a "firm connection of processed semiconductor wafers as a system wafer" refers to. It is unclear if there is an electronic structure covered by a cover wafer. It is unclear what "in an operation of a mechanically firm connecting electrically insulating connections and electrically conductive connections are produced between the semiconductor wafers" means, as it appears that multiple words may be missing.

Furthermore, the claim contains the limitation "applying a first electrically non-conducting, structure layer and a second electrically conducting layer of respectively one glass paste on at least one of the two wafers". The use of the word "respectively" in this case makes it ambiguous as to if one, or both, or the (1) electrically non-conducting layer" and (2) the electrically conducting layer" are formed, and if one or both are formed on either (a) one of, or (b) both of the wafers. It is also unknown how both layers (1) or (2) as listed above can be formed "respectively" from "one glass paste".

Furthermore, the limitation seems to imply one glass paste from the limitation "applying a first... layer... and a second... layer of respectively one glass paste" on lines 7-8 but seems to imply multiple glass pastes on lines 10 and 13 by use of the limitation "glass pastes". This contributes to the ambiguity described in the previous paragraph.

Lastly, the terms "processed semiconductor wafers", "system wafer", "cover wafer", "semiconductor wafers", "two wafers", and "the wafers" are all used in claim 11. It is unknown if they all refer to the same wafers, or if some of them refer to other

wafers. Thus, it is unknown how many wafers there are total or if all of them must be semiconducting.

Claims 12-19 depend from claim 11, and thus inherit its deficiencies. The "wafers" and "glass pastes" occur in claims 12-19, and should be brought into unambiguous agreement with the use of "wafer" and "paste" in claim 11.

20. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20 recites the limitation "for the firm connection of processed semiconductor wafers thereby connecting system wafers (1) supporting microelectromechanical or electronic structures (3) with cover wafers (2) wherein in an operation of a mechanically firm connecting both electrically insulating connections and electrically conducting connections are produced between the semiconductor wafers". The metes and bounds of the claimed limitation can not be determined for the following reasons: it is unknown what "wherein in an operation of a mechanically firm connecting both electrically insulating connections and electrically conducting connections are produced" means.

Furthermore, the limitation "applying structure layers or electrically non-conducting and electrically conducting glass pastes on respectively one of the two wafer sides to be connected with each other" is ambiguous. It is unknown how two pastes can "respectively" be formed on "one" side. Thus, it is unknown if one of, or both of, the

electrically non-conducting paste and the electrically conducting paste are formed on either one of, or both of, the two wafer sides.

Lastly, the terms "processed semiconductor wafers", "system wafers", "cover wafers", "semiconductor wafers", "two wafers", and "the wafers" are all used in claim 20. It is unknown if they all refer to the same wafers, or if some of them refer to other wafers. Thus, it is unknown how many wafers there are total or if all of them must be semiconducting.

21. In light of the aforementioned rejections of the claim(s) under 35 U.S.C. 112, second paragraph, the subsequent rejections under 35 U.S.C. 102 and/or 103 are based on prior art that reads on the interpretation of the claim language of the instant application as best understood by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

22. Claims 1-8, 11-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vanfleteren et al. (US 6,555,414 B1, hereinafter "Vanfleteren") in view of Kellar et al. US 2004/0142540 A1, hereinafter "Kellar").

Re claim 1, Vanfleteren discloses a process for the firm connection of processed semiconductor wafers **3** ("substrate" column 6, line 39) and **1** (alternatively called a "chip" column 6, line 41 and a "semiconductor chip", column 3, lines 51-55) wherein, in the case of more than two wafers, the wafers located in a central area of the stack and wherein in an operation of a mechanically firm connecting electrically insulating connections (**5** provides electrically non-conducting, or insulating, connection, Fig. 4C) and electrically conductive connections (**6** provides electrically conductive connection, Fig. 4C) are produced between the semiconductor wafers, said process comprising at least the following operations:

- applying structured layers of electrically non-conducting **5** (column 8, line 48 and Fig. 4C) and electrically conducting **6** (column 8, line 54 and Fig. 4B) glass paste (the electrically conducting adhesive is an "isotropically conducting adhesive", or ICA, which has a "glass transition temperature", column 8, line 29) on respectively one of the two wafer sides (both **5** and **6** are formed on the top side of the substrate **3**, Fig. 3C; the other side is the bottom side of IC chip **1**, Fig. 4E; **5** and **6** can further be said to be formed "on" the bottom side of **1**, because **1** and **3** are joined together, see Fig. 4F) to be connected with each other;
- conditioning and premelting (a "drying" process is conducted at 100 degrees; see column 8, lines 28-38; this occurs before curing, as can be considered "premelting" since "premelting" is not a recognized term, and could either mean "melting before" but "before what" isn't specified, or it could

mean some heating that occurs before "melting" or "curing") of the glass pastes;

- geometrical alignment (evolution from Fig. 4E to Fig. 4F) of the wafers to be connected; and
- joining (column 9, line 36 and evolution of Fig. 4E to 4F) of the wafers at a processing temperature (column 9, lines 40-41) of the glasses of glass pastes using a mechanical pressure (column 9, line 39).

Re claim 1, Vanfleteren fails to disclose joining two semiconducting wafers. It is noted that the "applying...", "conditioning...", "geometrical alignment...", and "joining..." steps, the wafers that are processed are not claimed to be semiconducting. It is reasonable that the preamble is discussing joining a semiconducting wafer to another wafer, which may or may not be semiconducting. Vanfleteren discloses the second option, as the substrate **3** can be a printed circuit board, transparent substrate, polyimide, or ceramic.

Kellar discloses bonding together multiple semiconducting wafers (paragraph 5) such as "active device wafers" (paragraph 18) with a "bonding adhesive such as borophosphosilicate glass (BPSG)" (paragraph 18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Kellar to the invention of Vanfleteren. The motivation to do so is that the combination produces the predictable results of bonding semiconducting wafers (Mori, paragraph 5).

Re claim 2, Vanfleteren further discloses that the glass pastes, in particular glass solders are applied with a screen printing process (column 7, line 58, wherein the conductive adhesive is screen printed).

Re claim 3, Vanfleteren further discloses that the non-conducting, low-melting glass paste (column 8, lines 50-54) and the electrically conducting glass paste (column 8, lines 27-31 and 45-47) have different conditioning and premelting conditions and that, consequently, the conditioning and premelting are implemented successively in a respectively separate process.

Re claim 4, Vanfleteren further discloses that the non-conducting, low-melting glass paste and the electrically conducting glass paste have substantially the same processing temperature (column 9, lines 36-45).

Re claim 5, Vanfleteren further discloses that the low-melting glass paste and the electrically conducting glass paste have different processing temperatures and these are successively passed in a process (column 9, lines 49-63).

Re claim 6, Vanfleteren further discloses that at least one of the wafers is electrically connected in an area that is not structured electronically as (an area of the starting material) (the wafer is connected between solder pads through adhesive 5, Fig. 4F).

Re claim 7, Vanfleteren further discloses that the wafers are electrically connected at specific switching points in electronically structured areas (the wafers are connected at solder pads 2A, see Fig. 4F).

Re claim 8, Vanfleteren further discloses that the formation of the connections of the glass pastes takes place at a temperature of less than 450°C (column 7, lines 64-65, column 8, lines 27-28, and column 9, lines 50-63).

Re claim 11, Vanfleteren discloses a process for the firm connection of processed semiconductor wafers as system wafer **1** supporting microelectromechanical or electronic structures with a cover wafer **3** also supporting electronic structures, wherein in an operation of a mechanically firm connecting electrically insulating connections (in **5**) and electrically conductive connections (in **6**) are produced between the semiconductor wafers, said process comprising at least the following steps:

- applying a first electrically non-conducting, structured layer **5** (column 8, line 48 and Fig. 4C) and a second electrically conducting layer **6** (column 8, line 54 and Fig. 4B) of respectively one glass paste (the electrically conducting adhesive is an "isotropically conducting adhesive", or ICA, which has a "glass transition temperature", column 8, line 29, and is thus "one glass paste") on at least one (both **5** and **6** are formed on the top side of the substrate **3**, Fig. 3C; the other side is the bottom side of IC chip **1**, Fig. 4E; **5** and **6** can further be said to be formed "on" the bottom side of **1**, because **1** and **3** are joined together, see Fig. 4F) of the two wafers to be connected with each other;
- conditioning (a "drying" process is conducted at 100 degrees; see column 8, lines 28-38; this occurs before curing) of the glass pastes;

- geometrical alignment (evolution from Fig. 4E to Fig. 4F) of the wafers to be connected;
- joining (column 9, line 36 and evolution of Fig. 4E to 4F) of the wafers at a processing temperature (column 9, lines 40-41) of the glass pastes using a mechanical pressure (column 9, line 39).

Re claim 11, Vanfleteren fails to disclose joining two semiconducting wafers. It is noted that the "applying...", "conditioning...", "geometrical alignment...", and "joining..." steps, the wafers that are processed are not claimed to be semiconducting. It is reasonable that the preamble is discussing joining a semiconducting wafer to another wafer, which may or may not be semiconducting. Vanfleteren discloses the second option, as the substrate **3** can be a printed circuit board, transparent substrate, polyimide, or ceramic.

Kellar discloses bonding together multiple semiconducting wafers (paragraph 5) such as "active device wafers" (paragraph 18) with a "bonding adhesive such as borophosphosilicate glass (BPSG)" (paragraph 18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Kellar to the invention of Vanfleteren. The motivation to do so is that the combination produces the predictable results of bonding semiconducting wafers (Mori, paragraph 5).

Re claim 12, Vanfleteren discloses that the glass pastes are glass solders (taken to mean "connectors", given the ambiguity as to its meaning as described above in a

112 2nd paragraph rejection) and are applied with a screen printing process (column 7, line 58, wherein the conductive adhesive is screen printed).

Re claim 13, Vanfleteren further discloses that the non-conducting, low-melting glass paste (column 8, lines 50-54) and the electrically conducting glass paste (column 8, lines 27-31 and 45-47) have one of different conditioning and/or premelting conditions and that, consequently, the conditioning and premelting of each of the pastes is implemented successively in a respectively separate process.

Re claim 14, Vanfleteren further discloses that the non-conducting, low-melting glass paste and the electrically conducting glass paste have substantially the same processing temperature (column 9, lines 36-45).

Re claim 15, Vanfleteren further discloses that the low-melting glass paste and the electrically conducting glass paste have different processing temperatures and these are successively passed in a process (column 9, lines 49-63).

Re claim 16, Vanfleteren further discloses that at least one of the wafers is electrically connected in an area that is not structured electronically as (an area of the starting material) (the wafer is connected between solder pads through adhesive 5, Fig. 4F).

Re claim 17, Vanfleteren further discloses that at least one of the wafers is electrically connected at specific switching points in an electronically structured area (the wafers are connected at solder pads **2A**, see Fig. 4F).

Re claim 18, Vanfleteren further discloses that the formation of the connections of the glass pastes takes place at a temperature of less than 450°C (column 7, lines 64-65, column 8, lines 27-28, and column 9, lines 50-63).

Re claim 20, Vanfleteren discloses a process for the firm connection of processed semiconductor wafers **3** ("substrate" column 6, line 39) and **1** (alternatively called a "chip" column 6, line 41 and a "semiconductor chip", column 3, lines 51-55) thereby connecting system wafers **1** (alternatively called a "chip" column 6, line 41 and a "semiconductor chip", column 3, lines 51-55) supporting microelectromechanical or electronic structures with cover wafers **3** ("substrate" column 6, line 39) wherein in an operation of a mechanically firm connecting both electrically insulating connections (**5** provides electrically non-conducting, or insulating, connection, Fig. 4C) and electrically conducting connections (**6** provides electrically conductive connection, Fig. 4C) are produced between the semiconductor wafers, having the steps:

- applying structured layers of electrically non-conducting **5** (column 8, line 48 and Fig. 4C) and electrically conducting **6** (column 8, line 54 and Fig. 4B) glass pastes (the electrically conducting adhesive is an "isotropically conducting adhesive", or ICA, which has a "glass transition temperature", column 8, line 29) on respectively one (both **5** and **6** are formed on the top side of the substrate **3**, Fig. 3C; the other side is the bottom side of IC chip **1**, Fig. 4E; **5** and **6** can further be said to be formed "on" the bottom side of **1**, because **1** and **3** are joined together, see Fig. 4F) of the two wafer sides to be connected with each other;

- conditioning and premelting (a "drying" process is conducted at 100 degrees; see column 8, lines 28-38; this occurs before curing, as can be considered "premelting" since "premelting" is not a recognized term, and could either mean "melting before" but "before what" isn't specified, or it could mean some heating that occurs before "melting" or "curing") of the glasses;
- geometrical alignment (evolution from Fig. 4E to Fig. 4F) of the wafers to be connected;
- joining (column 9, line 36 and evolution of Fig. 4E to 4F) the wafers at a processing temperature (column 9, lines 40-41) of the glasses pastes using a mechanical pressure (column 9, line 39).

Re claim 20, Vanfleteren fails to disclose joining two semiconducting wafers. It is noted that the "applying...", "conditioning...", "geometrical alignment...", and "joining..." steps, the wafers that are processed are not claimed to be semiconducting. It is reasonable that the preamble is discussing joining a semiconducting wafer to another wafer, which may or may not be semiconducting. Vanfleteren discloses the second option, as the substrate 3 can be a printed circuit board, transparent substrate, polyimide, or ceramic.

Kellar discloses bonding together multiple semiconducting wafers (paragraph 5) such as "active device wafers" (paragraph 18) with a "bonding adhesive such as borophosphosilicate glass (BPSG)" (paragraph 18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Kellar to the invention of Vanfleteren. The

motivation to do so is that the combination produces the predictable results of bonding semiconducting wafers (Mori, paragraph 5).

23. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vanfleteren and Kellar as applied to claims 1 and 11 above, and further in view of Christensen et al. (US 2003/0170936 A1, hereinafter "Christensen").

Re claims 9 and 19, Vanfleteren discloses the limitations of claims 1 and 11, as discussed above, but fails to further disclose the process according to claim 1 and any of the subsequent claims, "characterized in" that the electric connection of the substrate for SOI wafers is implemented through previously produced openings in a buried oxide layer and in an active silicon layer, in particular the wall areas of the opening of the active silicon layer being provided with an insulating layer prior to the electric connection (claim 9) with the conducting glass solder (claim 19). Christensen discloses that the electric connection of the substrate for SOI wafers (paragraph 2) is implemented through previously produced openings **300** (Fig. 3 and paragraph 24) in a buried oxide layer **106 or 108** (Fig. 3) and in an active silicon layer **102** (Fig. 3), "in particular" the wall areas of the opening of the active silicon layer being provided with an insulating layer **400** (Fig. 4) prior to the electric connection. It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Christensen to the invention of Vanfleteren. The motivation to do so is that the combination produces the predictable results of connecting a SOI wafer with improved speed of signals (Christensen paragraph 2) to an external wafer (Vanfleteren).

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Parendo, whose can be contacted by phone at (571) 270-5030 or directly by fax at (571) 270-6030. The examiner can normally be reached on Mon.-Thurs. and alternate Fridays from 7 a.m. - 4:30 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kevin A. Parendo/

Examiner, Art Unit 2823
12/18/2008

/Hsien-ming Lee/

Primary Examiner, Art Unit 2823